

## **REMARKS**

Claims 1-4, 6-12 and 15-22 are pending in the application. The Examiner's reconsideration of the rejections in view of the amendments and remarks is respectfully requested.

Applicants appreciate the examiner's indication that Claims 3, 5-7, 10, 12-17 and 20 would be allowable if rewritten to overcome the rejections under 35 USC 112, 2<sup>nd</sup> paragraph, set forth in the Office Action and to include all of the limitations of the base claim and any intervening claims.

The drawings have been objected to – the examiner suggested that FIGS. 1-4 be designated as “Prior Art.” Replacement sheets depicting FIGS. 1-4 as prior art are attached. Reconsideration of the objection is respectfully requested.

The specification has been objected to for various informalities. Applicants appreciate the examiner's suggested amendments. A substitute specification, including the abstract of the invention, is attached hereto. The substitute specification includes no new matter.

Claims 3, 7, 10, and 20 have been rejected under 35 USC 112, first paragraph, as being based on a disclosure that is not enabling. The examiner stated essentially that a vector  $s(x)$  calculated from the cumulative vector is not enabled.

Respectfully, applicants point to page 10, line 28 to page 11, lines 4, as teaching a cumulative vector. Further,  $s(x)$  is taught as a permutation sequence at page 12, lines 6-8. Thus,

the vector calculated from the cumulative vector is a permutation sequence. One of ordinary skill in the art would recognize how to calculate such a vector from the cumulative vector in view of the disclosure. Reconsideration of the rejection is respectfully requested.

Claims 1-20 have been rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the examiner suggested amendments to Claims 1-4, 7-11, 15, 16 and 18-20.

Claims 1-4, 7-11, 15, 16 and 18-20 have been amended in view of the examiner's suggested amendments. Reconsideration of the rejection is respectfully requested.

Claims 1, 2, 18 and 19 have been rejected under 35 USC 102(e) as being anticipated by Kim (USPN 6,721,908). The examiner stated essentially that Kim teaches all the limitations of Claims 1, 2, 18 and 19.

Claim 1 claims, *inter alia*, "an address generator means for generating an interleaved address on the fly using the seed variables and performing an add operation." Claim 18 claims, *inter alia*, "generating interleaved addresses column by column using the seed variables and performing an add operation."

Kim teaches a turbo coder including an interleaver (see col. 1, lines 25-27). Kim does not teach "an address generator means for generating an interleaved address on the fly using the seed variables and performing an add operation" as claimed in Claim 1 nor "generating interleaved addresses column by column using the seed variables and performing an add operation" as claimed in Claim 18. Kim's interleaving device includes a multiplexer, which selects an output

of PN generators according to a select signal provided from a counter, and a subtracter (see col. 15, lines 59-63). Kim's interleaving device does not include an adder - Kim does not teach that the generation of an interleaved address uses seed variables and performing an add operation, as claimed in Claims 1 and 18. Therefore, Kim fails to teach all the limitations of Claims 1 and 18. Claims 1 and 18 are believed to be in condition for allowance.

Claims 2 and 19 depend from Claims 1 and 18, respectively. The dependent claims are believed to be allowable for at least the reasons given for the respective independent claims. The examiner's reconsideration of the rejection is respectfully requested.

Claims 4, 8, 9 and 11 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Zhou et al. (USPN 7,058,874). The Examiner stated essentially that Zhou teaches or suggests all the limitations recited in Claims 4, 8, 9 and 11.

Claims 4 and 8 have been amended to include the allowable limitations of Claims 5 and 13, respectively. Therefore, Claims 4 and 8 are believed to be in condition for allowance. More particularly, Zhou does not teach or suggest "generated interleaved address is once stored in the address queue and reused as a write address for writing the log likelihood ratio outputted from the SISO decoder into the LLR memory" as claimed in Claim 4, nor "wherein the processor is a single-instruction multiple-data (SIMD) processor" as claimed in Claim 8.

Referring to Claim 4, Zhou teaches a log-likelihood ratio (LLR) of probabilities (see col. 1, lines 59-61). Zhou is silent on the writing of the LLR of probabilities. Therefore, Zhou fails to teach or suggest that a generated interleaved address is reused as a write address for writing the log likelihood ratio, essentially as claimed in Claim 4.

Referring to Claim 8, Zhou teaches only a digital signal processor (DSP) (see col. 9, lines 54-55) – nowhere does Zhou teach or suggest that the DSP is a SIMD processor.

Therefore, Zhou fails to teach or suggest all the limitations of Claims 4 and 8. Claims 9 and 11 depend from Claim 8. The dependent claims are believed to be allowable for at least the reasons given for Claim 8. The examiner's reconsideration of the rejection is respectfully requested.

Claims 21 and 22 include the limitations of Claim 1 and allowable Claim 3, and Claim 18 and allowable Claim 20, respectively. Therefore, Claims 21 and 22 are believed to be in condition for allowance.


For the forgoing reasons, the application, including Claims 1-4, 6-12 and 15-22, is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

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